157 nm Resist Evaluation and Process Development at Intel

Jeanette Roberts, John Hutchinson, Baohua Niu, Lee Rockford, Eric Panning, Raghu Balasubramanian, Janet Chambers, and Jim Powers

Components Research – Intel Corporation

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Introduction

- **Goal of Intel's 157nm Resist Program:**
  - Develop 157nm resist processes to allow development of the 70nm node starting in 2003 and high-volume manufacturing in 2005

Enable Technology, Remove Showstoppers		Integrate Components, Develop Manufacturable Process		High Volume Manufacturing Across Multiple Factories	
2001	**2002**	**2003**	**2004**	**2005**	**2006**

Intel Strategy

- **Intel is obtaining imaging capability in three phases**
  - I: Microstepper,'99
    - 0.5 NA, 0.3 σ, 100 μm diameter field
    - Provides a way to screen resists
  - II: The first 157nm mid-field tool, '01
    - 0.75 NA, 0.8 σ, 4 x 22 mm field size
  - III: Full field exposure tool

- **Intel is also leveraging International SEMATECH exposure capability**
  - Q3'00 Sematech accepted 157nm exposure tool
    - 0.6 NA, 1.5 x 1.5 mm field size

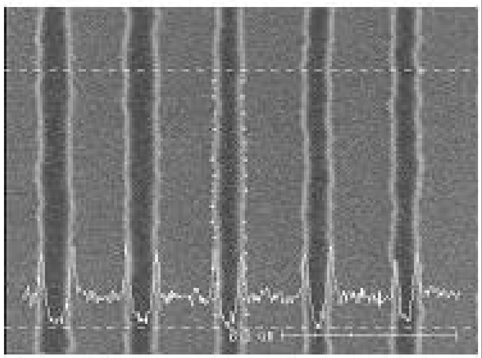
Present Status

- **Resists for 157 nm have made significant progress over the last year**
  - Hundreds of photoresists have been screened
  - Two methods for increasing transparency are producing encouraging results
    - Si based resists
    - Fluorinated resists
  - More resist suppliers are actively developing resists for 157nm
  - Resists from several vendors meet some targets (e.g., depth of focus and dose sensitivity)
  - All resists must improve (e.g., line-edge roughness, thickness, and imaging on non-reflective substrates)

Improved Imaging Over Last Year

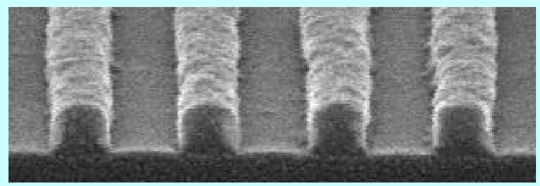
- **Resist thickness: 2-3X increase**
- **Resolution: ~ 40% improvement**
- **Imaging on absorbing substrates**

March 2000

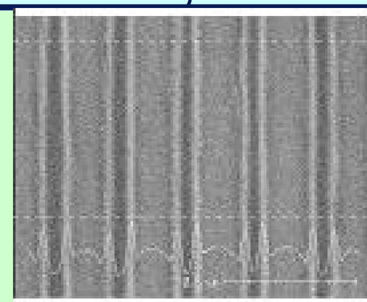


88nm (~ 1:2)
577 Å, on Si

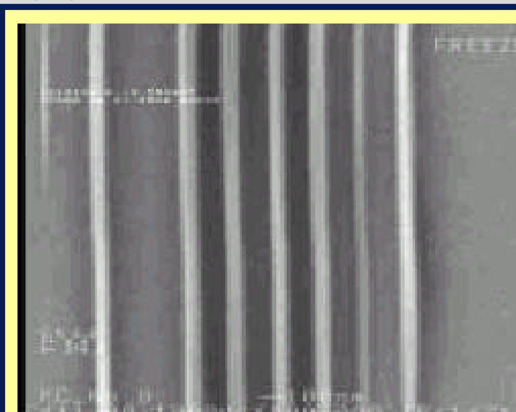
May 2001



90nm (1:1)
790 Å, on Si



100nm (1:1.5)
1025 Å, on SiON



80nm (1:1)
1560 Å, on Si

Resist Evaluation Matrix

- **Basic lithographic performance is being tracked**
- **Additional requirements are critical, but will not be discussed here, including:** plasma etch resistance, outgassing, adhesion, sidewall angle, defects, isolated line and contact criteria, etc

Attribute	ITRS (70nm)
Substrate*	Si, SiON
Thickness, imaging layer (nm)	210-280
Photospeed (mJ/cm2)	10
Half-pitch (nm)	80
DOF (nm)	500
Dose Sensitivity* %	10%
LER* (nm, 3s)	4

*** Not in ITRS**

Vendor Comparison

- Improvements must be made by all resists in thickness and LER
- Imaging is typically much worse on SiON compared to Si
- Criteria will be added as improved imaging allows

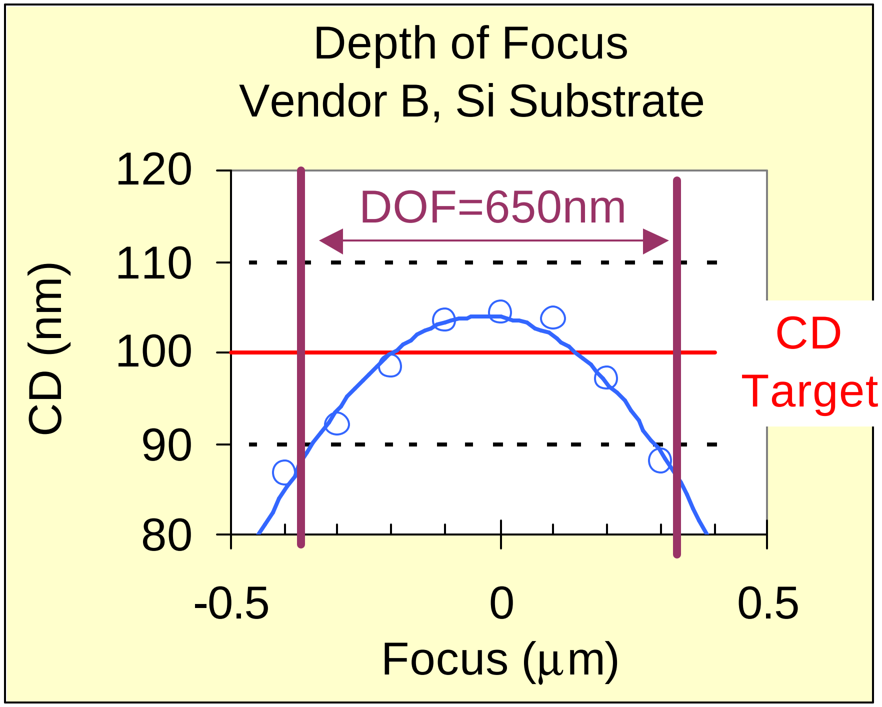
Attribute	ITRS (70nm)	Vendor A		Vendor B		Vendor C	
Substrate		Si	SiON	Si	SiON	Si	SiON
Thickness, imaging layer (nm)	210-280	68	68	101	101	120	120
Photospeed (mJ/cm2)	10	1.5	1.8	7.6	9	30.5	33.8
Half-pitch (nm)	80	90	90	90	90	90	90
DOF (nm)	500	1000	200	700	100		500
Dose Sensitivity* %	10%	12%	8%	8%	2%		1%
LER* (nm, 3s)	4	9	15	9	11		9

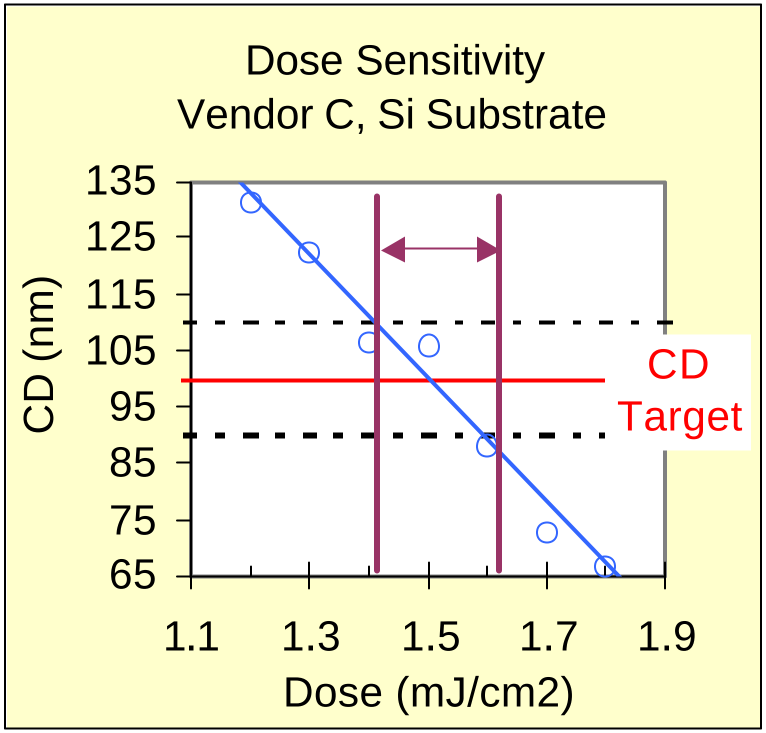
* Not in ITRS

color code:
- Meets
- Exposure Tool Limited
- Does Not Meet

Typical DoF and Dose Sensitivity Data

- Most resists have adequate DOF and Dose Sensitivity, as measured on the Intel microstepper (PSM)
- Depth of Focus and Dose Sensitivity are measured using 100nm lines, ±10%, on 250 nm pitch



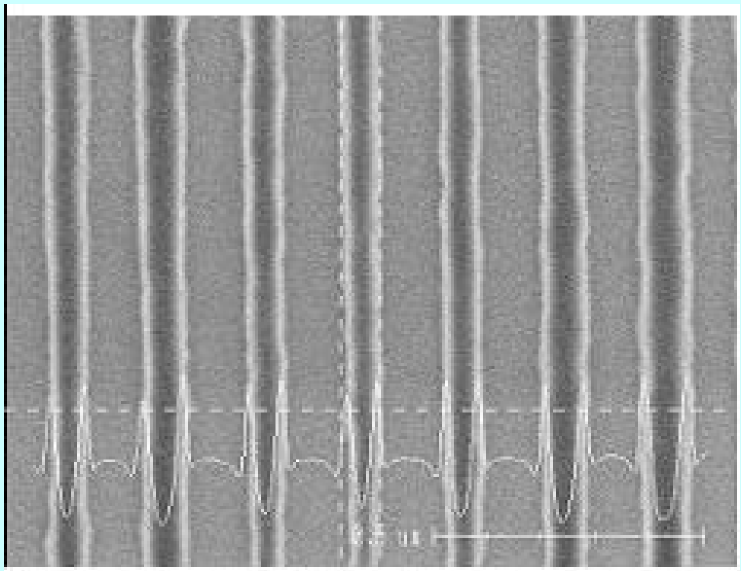


Resist Evaluation on Different Substrates

- Poor imaging on SiON substrates is common
- 157nm production resists will need to function with multiple substrates (SiON, SiO2, etc.)

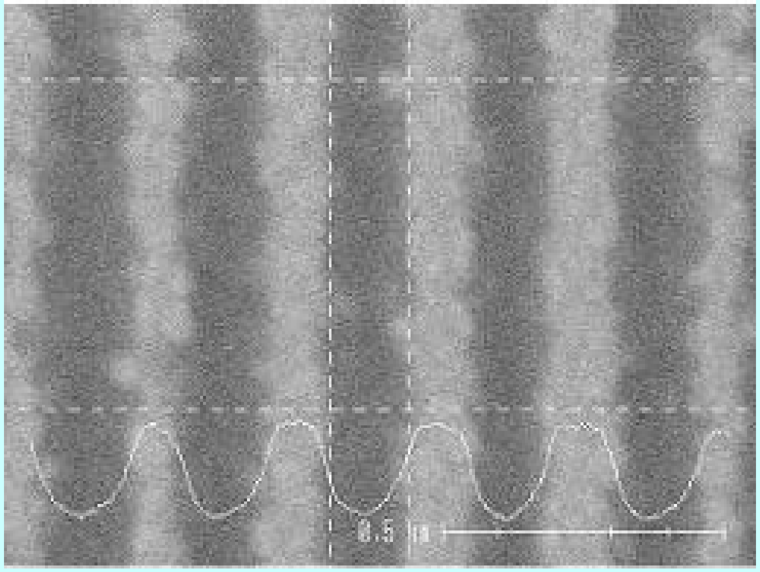
Resist A

80 nm Thick Resist



Si Substrate

180 nm pitch (100kX)



SiON substrate

250 nm pitch (100kX)

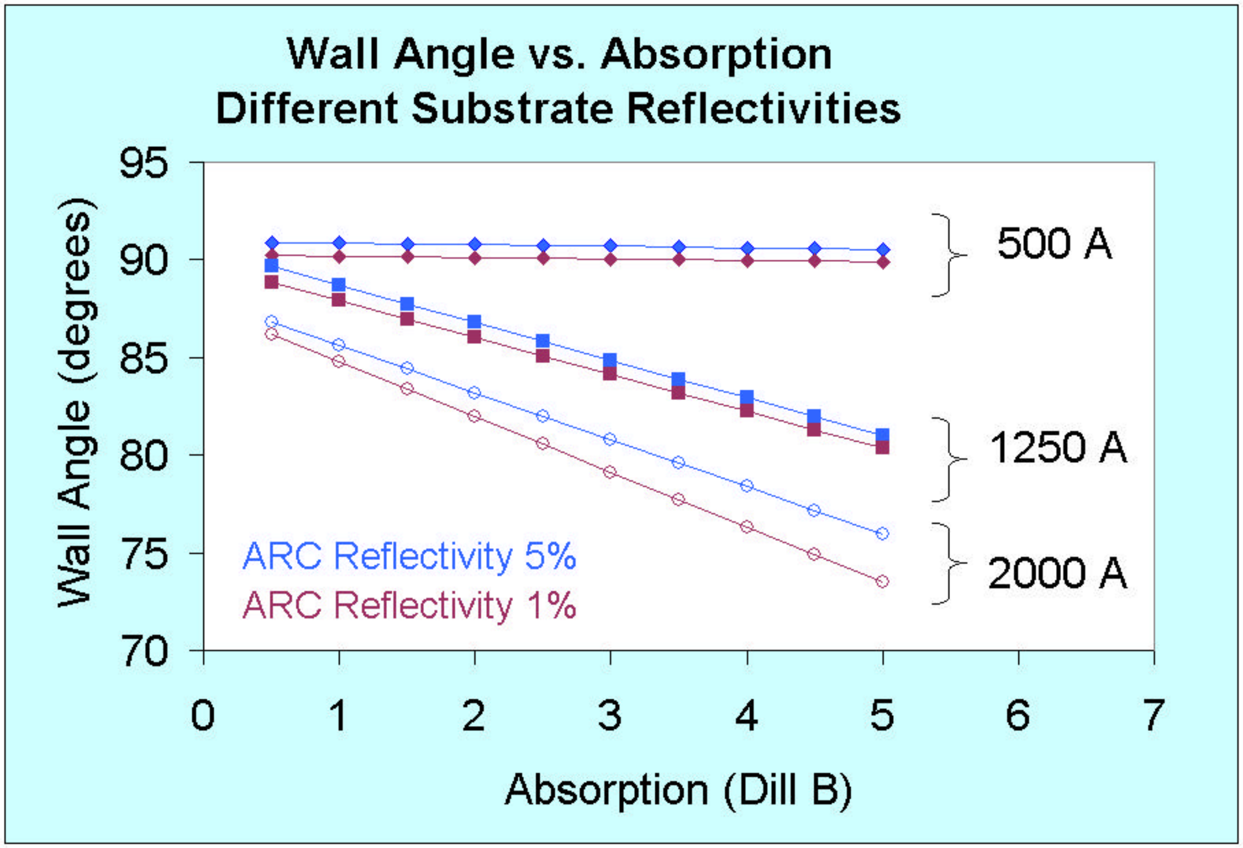
Absorbance Requirements: modeling data

- **A key challenge in 157 nm resist development is the identification of a polymer sufficiently transparent to produce steep sidewall angles and acceptable CD control**

- **Simulations were done to estimate the acceptable absorbance range for different resist thicknesses on various substrates**
  - Used Intel internally developed software
  - Adapted the 193 nm poly resist model to 157 nm
  - Fixed: λ=157 nm, NA = 0.75, σ = 0.75, 4X reduction
  - Used 70 nm isolated lines
  - Mask: binary mask with 140 nm chrome (2X bias)
  - Used Anti-reflective Coating (ARC) and Si substrates

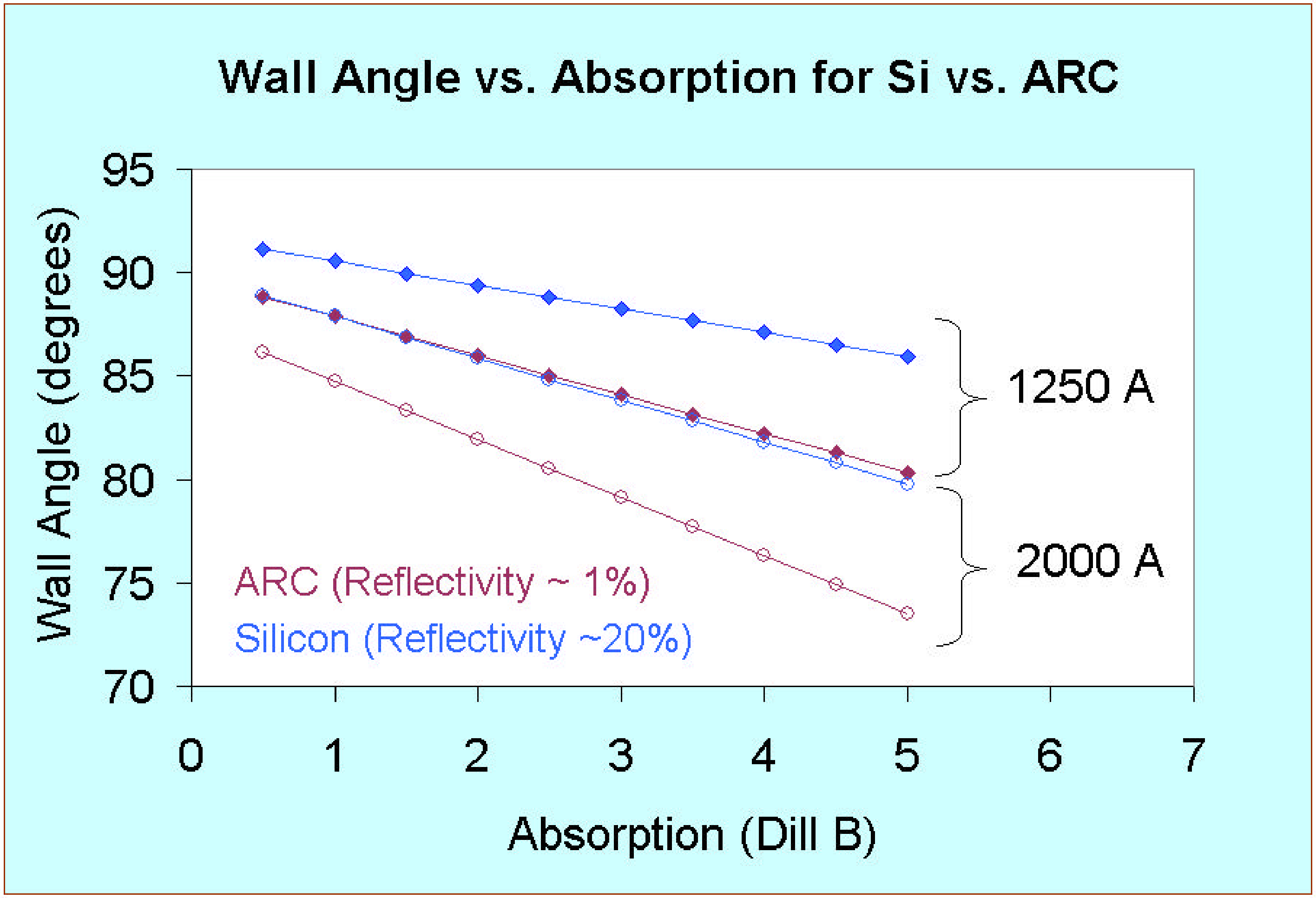
Resist Simulations:
ARC reflectivity, resist thickness, and absorbance

- A detuned ARC compared to an optimized ARC improves resist wall angle by only a small amount ~0.5° - 1.5°
- For thick resists, small changes in absorbance results in large angle changes



Resist Simulations: Si vs ARC

- Resist characterizations should be done on absorbing substrates to truly demonstrate resist performance



Summary / Conclusions

- **Intel is actively characterizing and developing 157nm resists for the development of the 70nm node beginning in 2003**
  - We are actively engaged with several resist suppliers
  - Much progress has been made over the last year
    - Resist thickness increased by 2-3X
    - Resolution improved by ~40%
  - Areas for improvement include
    - Resist thickness, LER, imaging on non-reflective substrates
  - For thick resists, small changes in absorbance results in large changes in resist wall angle
    - Therefore we need as much transparency as we can get!

Acknowledgements

- The resist suppliers, for developing resists for 157nm
- Our colleagues and management including Susan Holl and Jerry Marcyk
- The staff at International SEMATECH for their support

Backup

Complete Evaluation Matrix

Attribute	ITSR (70nm)	Vendor A'		Vendor B'		Vendor C'		Vendor D'		Vendor E'	
Substrate		Si	SiON	Si	SiON	Si	SiON	Si	SiON	Si	SiON
imaging layer (nm)	210-280	79	79	85	85	68	68	101	101	120	120
Thickness UTR (nm)	100-150	79	79	85	85	68	68	101	101	120	120
Photospeed (mJ/cm2)	10	2.8	2.9	2.5	3.9	1.5	1.8	7.6	9	30.5	33.8
Half-pitch (nm)	80	90	90	90	90	90	90	90	90	90	90
DOF (nm)	500	800	600	650	350	1000	200	700	100		500
Dose Sensitivity* %	10%	10%	10%	10%	12%	12%	8%	8%	2%		1%
LER* (nm, 3s)	4	8	10	8		9	15	9	11		9

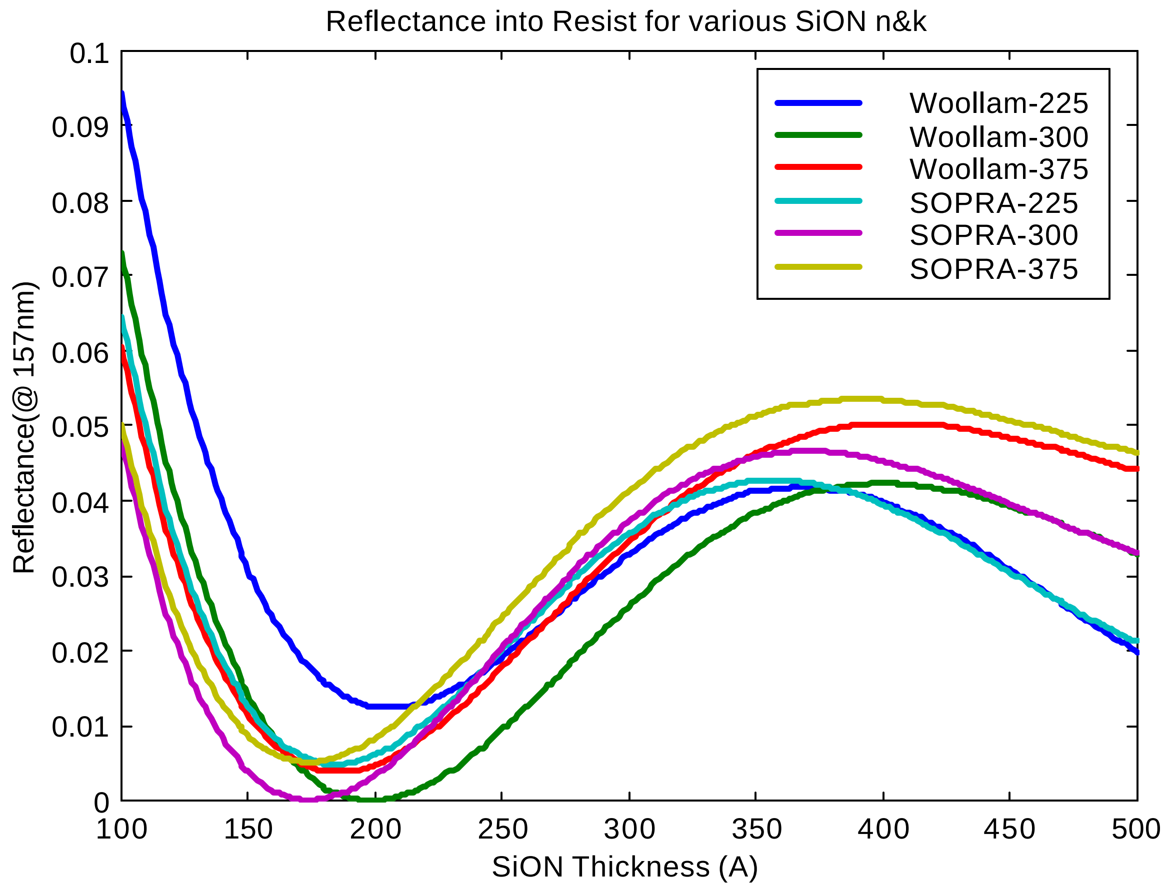
* Not in ITSR

color code:
- Meets
- Exposure Tool Limited
- Within Target Range
- Does Not Meet

Comparison of Exposure Tools

Feature	Intel Microstepper	SEMATECH Microstepper	Intel Miniscanner targets
Tool Optics	Schwarzschild reflecting objective reduced obscuration design	Modified catadioptric design	Modified catadioptric design similar to SEMATECH
Max Field Size	< 70 μm x 70 μm	1.5 mm x 1.5 mm	4 mm x 22 mm (4mm x 4mm static)
NA	0.5	0.6	**0.75**
σ [partial coherence]	0.3, typically (variable)	0.7, 0.2, (variable)	**0.8 (variable)**
Cross-field Dose Uniformity	Target 10% at maskplane; actual is much worse	< 10% (except at the reticle edge)	**< ±1.5%**
Resolution	180nm pitch (1:1) alt-PSM		At least 200nm pitch (1:1) binary; (~ 30% improvement over SEMATECH design)
Magnification	36X	10X	6X

ARC Reflectivity vs. Thickness



Used 200A for low reflectance case (~1%)
Used 375A for high reflectance case (~4.5%)

Depth of Focus Data

- For plot on page 9